SB16C554PL / SB16C554TQ

QUAD-UART
ASYNCHRONOUS COMMUNICATION ELEMENT

Introduction

SB16C554PL/SB16C554TQ is an enhanced quadruple version of the 16C550 UART(Universal Asynchronous Receiver Transmitter). Each channel can be put into FIFO mode to relieve the CPU of excessive software overhead. In this mode, internal FIFOs are activated and 16 bytes plus 3 bits of error data per byte can be stored in both receive and transmit modes.

Each channel performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. The Status information includes the type and condition of the transfer operations being performed by the UART as well as any error conditions such as parity, overrun, framing and break interrupt.

SB16C554PL/SB16C554TQ includes a programmable baud rate generator which is capable of dividing the timing reference clock input by divisors of 1 to $2^{16}-1$ and producing a $16 \times$ clock for driving the internal transmitter logic. Provisions are also included to use this clock to drive the receive logic.

SB16C554PL/SB16C554TQ has complete MODEM-control capability and an interrupt system that can be programmed to the user's requirement, minimizing the computing required to handle the communication links.

Features

- In the FIFO mode, Each channel's transmitter and receiver is buffered with 16 byte FIFO to reduce the number of interrupts to CPU.
- Adds or deletes standard asynchronous communication bits(start, stop, parity) to or from the serial data.
- Holding Register and Shift Register eliminate needs for the precise synchronization between the CPU and serial data.
- Independently controlled transmit, receive, line status and data interrupts.
- Programmable Baud Rate Generators which allow division of any input reference clock by 1 to $2^{16}-1$ and generate an internal $16 \times$ clock.
- Independent receiver clock input.
- Modem control functions(RTS#, CTS#, DTR#, DSR#, DCD# and RI#).
- Fully programmable serial interface characteristics.
    - . 5, 6, 7 or 8 bit characters.
    - . Even, Odd, No parity bit
    - . 1, 1.5, 2 Stop bit generation. (Like other general UARTs, SB16C554PL/SB16C5TQ 54TQ checks one stop bit, no matter how many they are)
- False start bit detection.
- Generates or Detects Line Break.
- Internal diagnostic capabilities : Loopback controls for comminication link fault isolation.
- Fully prioritized interrupt system controls.

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