SB16C554A

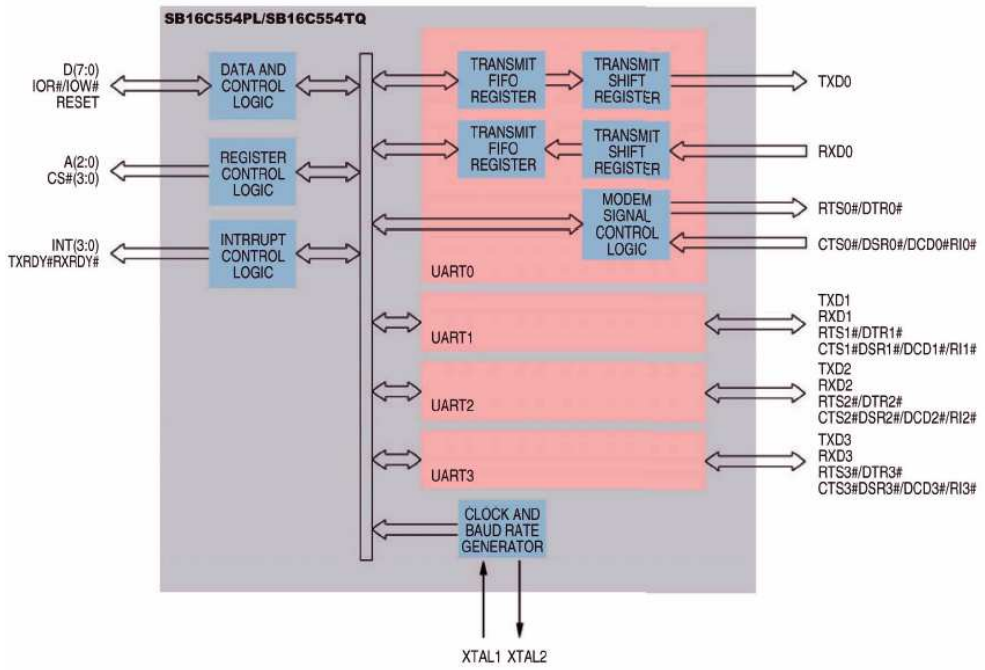
Quadruple Universal Asynchronous Receiver and Transmitter

SB16C554A is an enhanced quadruple version of the 16C550 UART(Universal Asynchronous Receiver Transmitter). Each channel can be put into FIFO mode to relieve the CPU of excessive software overhead. In this mode, internal FIFOs are activated and 16 bytes plus 3bits of error data per byte can be stored in both receive and transmit modes.

Each channel performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. The Status information includes the type and condition of the transfer operations being performed by the UART as well as any error conditions such as parity, overrun, framing and break interrupt.

SB16C554A has complete MODEM-control capability and an interrupt system that can be programmed to the user's requirement, minimizing the computing required to handle the communication links.

■ SB16C554A Features



■ SB16C554A Features

- **Integrated Four Improved SB16C550A UART**
- **In the FIFO mode, Each channel's transmitter and receiver is buffered with 16-byte FIFO to reduce the number of interrupts to CPU.**
- **Adds or deletes standard asynchronous communication bits(start, stop, parity) to or from the serial data.**
- **Holding Register and Shift Register eliminate needs for the precise synchronization between the CPU and serial data.**
- **Independently controlled transmit, receive, line status and data interrupts.**
- **Programmable Baud Rate Generators which allow division of any input reference clock by 1 to 2^{16}-1 and generated an internal 16x clock.**
- **Modem control functions (RTS#, CTS#, DTR#, DSR#, DCD# and RI#)**
- **Independent receiver clock input.**
- **Fully programmable serial interface characteristics.**
  - **5, 6, 7 or 8 bit characters.**
  - Even, Odd, No parity bit
  - 1, 1.5, 2 Stop bit generation.
  - Like other general UARTs, SB16C554A checks one stop bit, no matter how many they are.
- **False start bit detection and Generates or Detects Line Break.**
- **Internal diagnostic capabilities : Loopback controls for communication link Fault isolation.**
- **Fully prioritized interrupt system controls.**
- **Programmable Auto-RTS# and Auto-CTS#**
- **CTS# Controls Transmitter in Auto-CTS# Mode**
- **RCV FIFO Contents and Threshold Control RTS# in Auto-RTS# Mode**
- **3.3V Operation**
- **80-pin TQFP, 68-pin PLCC, 64-pin TQFP Packages**

■ SB16C554A Ordering Information

Products	Description
SB16C554A-TQ80	80-pin TQFP Package Quad-UART with 16-byte FIFOs
SB16C554A-TQ64	64-pin TQFP Package Quad-UART with 16-byte FIFOs
SB16C554A-PL68	68-pin PLCC Package Quad-UART with 16-byte FIFOs

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