IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2011 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 20, 21, 22, 23, 24

CONFERENCE THEME:

ELECTRONICS FOR HEALTHY LIVING

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

NEW THIS YEAR:
Plenary Roundtable
(in addition to 3 Plenary talks)
Industrial Demo Session

5-DAY PROGRAM

SUNDAY ALL-DAY: 2 FORUMS:
Transmitters for Wireless Infrastructure; ULV Circuits for Energy-Efficient Systems

9 TUTORIALS: nm Layout; SC Noise Analysis; Power-Delay Tradeoffs; Silicon-Body Interface; Digital - Ultra Low Voltage & Power; Embedded Memory; LC Oscillators; Rx Distortion; DPLL CDR

EVENING: 2 SPECIAL-TOPIC SESSIONS & STUDENT RESEARCH PREVIEW

THURSDAY ALL-DAY: 4 FORUMS:
Personalized Medical Care; Green Microprocessors; 3D Image Sensors; High-Speed Xceivers

SHORT-COURSE: Cellular and Wireless LAN Transceivers

26.5 A GPS/Galileo SoC with Adaptive In-Band Blocker Cancellation in 65nm CMOS **3:30 PM**

C-H. Wu[1], W-C. Tsai[1], C-G. Tan[2], C-N. Chen[1], K-I. Li[1], J-L. Hsu[1], C-L. Lo[1], H-H. Chen[1], S-Y. Su[1], K-T. Chen[1], M. Chen[1], O. Shana'a[2], S-H. Chou[1], G. Chien[3]
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A host-based GPS/Galileo SoC achieves 2.0dB NF, -165dBm chip-in tracking sensitivity, -5dBm out-of-band IIP3, and consumes 18mW (8.6mW for RF portion). The device can sustain out-of-band blockers as high as +16dBm at its antenna port without the need of external LNA and inter-stage SAW filter. By using the proposed scheme of in-band blocker cancellation, this SOC can withstand 12 in-band CW blockers simultaneously. The chip consumes 6.6mm^2 in a 65nm CMOS process.

26.6 A 0.05-to-10GHz 19-to-22GHz and 38-to-44GHz SDR Frequency Synthesizer in 0.13µm CMOS **3:45 PM**

S. Rong, H. Luong
HKUST, Hong Kong, China

An SDR frequency synthesizer covers not only all the wireless standards from 47MHz to 10GHz (including 14-band MB-OFDM UWB) but also the 802.15.3c standard from 57 to 66GHz. Implemented in a 0.13µm CMOS, the prototype occupies an active area of 3mm^2, consumes a total power of 33 to 83mW, and achieves a measured phase noise of -139.6dBc/Hz at 3MHz offset from a 1.7GHz carrier.

26.7 A 4.6GHz MDLL with -46dBc Reference Spur and Aperture Position Tuning **4:15 PM**

T. A. Ali[1,2], A. A. Hafez[1], R. Drost[2], R. Ho[2], C-K. Yang[1]
[1]University of California, Los Angeles, CA
[2]Oracle, Menlo Park, CA

An MDLL with aperture position tuning is presented. A calibration loop slides a phase interpolator and places the aperture in optimal position to minimize period jitter and spurs. A charge pump with static and dynamic mismatch is designed to minimize phase errors. The MDLL is implemented in a 90nm process. It achieves -46dBc of reference spur at 4.6GHz and consumes 6.8mW.

Conclusion **4:30 PM**